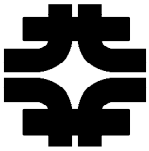

Fermi National Accelerator Laboratory

D-Zero Central Fiber Tracker
Analog Front End Board, Revision 2
(AFE II)

Design Specification

--PRELIMINARY--

July 30, 2002

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1. GENERAL INFORMATION

This document describes the design of the Analog Front End Board, Revision II (AFE II) which has the function of receiving charge signals from the Central Fiber Tracker and providing digital hit pattern and 8-bit charge amplitude information from those charge signals. The AFE digitizes 512 channels of information and provides one bit of discriminator data per input. Each input is also stored in an analog pipeline and, upon command, one of the selected pipeline values for each channel is digitized to eight bit resolution and read out.

The original AFE was designed for use in Run IIa of the D-Zero detector. The charge signal discrimination and A/D conversion was accomplished using the SIFT discriminator chip (designed by an outside consultant) and the SVX IIb A/D chip. Performance limitations of the SIFT render the extant AFE boards incapable of running at the faster interaction rates expected in Run IIb. The experiment has decided to replace the existing AFE boards with new ones that replace the SIFT/SVX combination by a new discriminator chip, the TRiP, and commercial A/D converters.

A great deal of software, test setup and system configuration has accompanied the rollout of the Central Fiber Tracker. While flaws in the SIFT require a redesign of this particular board for the faster interaction rate expected in Run IIb, there is no logical reason to allow the changes to bleed over into the rest of the system. Therefore, the general design specification of the AFE II is easily summarized:

The AFE II, a replacement for the AFE I to support 132 nsec operation, shall emulate the AFE I transparently for 396 nsec mode operation, such that an AFE II is completely indistinguishable from the AFE I to any external hardware interfaces, control software, sequences or procedures. The AFE II may implement additional commands or functions only when necessary to support 132 nsec operation or to support specific features of the TRiP chip not present in the SVX IIb, so long as any of these additions do not impact the AFE I emulation.

The remainder of this document shall pursue this general specification, specifically highlighting any changes which fail to meet the above goal.

1.1. Document Conventions

As might be expected, this document is much the same as the design specification of the AFE I. Unfortunately, other systemic issues encountered during the design and implementation of the Central Fiber Tracker have resulted in the AFE implementation drifting away from the original specification in order to provide solutions for other troubles in the system. Therefore, many statements made in the original release of this Design Specification are no longer valid due to changes in the system where the AFE resides. Examples of some of these major system changes are:

- The number of multi-chip-modules made available to mount onto the AFE boards was far less than the number expected. A 12-MCM variant of the AFE I was going to be made, but because insufficient MCMs were available, a larger number of 8-MCM AFE boards were manufactured instead and the 12-MCM design was halted before any boards were produced. The 12-MCM design had special logic for the Central Preshower detector which then had to be grafted into the 8-MCM AFE logic implementation.

- The original CFT system was supposed to drop the optical waveguides into the AFE cassettes in detector sector order, where each cassette would 'see' an entire sector. This was predicated on the development of an optical fiber patch panel which was never constructed. The waveguides were connected, not in sector order, but by fiber ribbon order. This necessitated the development of a whole new system – the Mixer – to re-scramble the discriminator data back into sector order prior to its delivery to the Digital Front Ends, or DFEs. Further fallout from this was the need to develop LVDS 'personalities' – 128 different versions of one of the CPLDs where originally only one was required.

Readers shall certainly wish to understand in detail how the AFE II differs from the AFE I. To keep the distinctions clear, the following text conventions shall be followed throughout this document:

- Sections of text that describe the CFT system *as it was at the time the AFE I was conceived*, but which no longer are valid, shall be marked with ~~strikethrough text~~ to indicate that these requirements and/or features are no longer valid in the as-built system.
- Added explanatory text delineating new or modified system requirements or conditions shall be highlighted by use of the following font: This is a systemic change.
- Sections of text that describe specifically how the AFE II is implemented *differently* than the AFE I shall be indicated by paragraphs which have a bold and obvious border surrounding them, e.g.:

This describes new implementations found in the AFE II that were not in AFE I.

1.2. System Introduction

The CFT system consists of a set of 8 concentric cylinders of optical fiber arranged in layers. Each of these layers has 'axial' fibers, that is, those which run parallel to the beam direction; there are also 'stereo' fibers, which wrap in gentle helices around the beamline. Half of the 'stereo' fibers have a clockwise twist, and the other half have a counter-clockwise twist, such that data from a correlated clockwise and counter-clockwise pair of hits indicates a distance from the interaction point along the beam axis. The 360 degrees of rotation around this axis have been broken into 80 'sectors', each of which spans 4.5 degrees~~. Each AFE board is connected to one sector's worth of fibers.~~ Each AFE board is connected to 512 fibers, typically two 'ribbons' containing all fibers of one layer in a contiguous group spanning some small fraction of the 360 degrees. Two boards are installed into a mechanical 'cassette', which views a total of 1024 fibers. The mechanical design of the cassette requires that the two boards be on opposite sides; part height clearances require that both boards face 'away' from the centerline of the cassette. This has resulted in the concept of 'right-handed' and 'left-handed' boards, indicative of the direction in which the components protrude away from the cassette centerline when viewed from the front. The AFE is implemented as a single 'non-handed' design – that is, a single layout which can be used in both orientations dependent on the installation or non-installation of certain components.

Each successive layer of fibers from innermost ('A') to outermost ('H') has more fibers than the last; in addition, an eighth layer of Preshower ('PS') fibers exists outside the H layer. Preshower fibers are larger than the axial fibers; there are relatively few PS fibers per sector, but triggering requirements force a different circuit design for PS fibers as opposed to axial fibers. ~~Every PS fiber is measured twice, at two different thresholds; also, the thresholds associated with the PS fibers are sufficiently different from the axial fibers that the entire PS circuit must be independent of any axial fiber circuit. This places limits on the distribution of fibers into the AFE boards.~~ The Preshower fibers generate significantly more charge than the Axial or Stereo fibers, so a smaller coupling capacitance is soldered to the AFE board for Preshower channels.

Each sector of information from the detector consists of 512 'axial' fibers and an additional 512 'stereo' fibers. Each sector contains

- 32 'A' layer fibers
- 40 'B' layer fibers
- 48 'C' layer fibers
- 56 'D' layer fibers
- 64 'E' layer fibers
- 72 'F' layer fibers
- 80 'G' layer fibers
- 88 'H' layer fibers
- 32 'PS' layer fibers

Only the 'axial' fibers are used in trigger formation, so all 'axial' fibers are routed into one set of AFE boards and all 'stereo' fibers are routed into different AFE boards. The Preshower is handled separately so there are 480 axial fibers per sector required to form the trigger. A second complication is that the Preshower fibers are further broken up along the beamline axis; at any given spot around the cylinder, the single Preshower location of that angle has two Central Preshower fibers – a Central North and a Central South. ~~To accommodate the dual threshold measurements required of Preshower fibers, the 12-MCM version of the AFE is used where eight of the twelve measurement blocks are utilized as four dual-threshold devices. The remaining four measurement devices are then used as single-threshold objects for some of the 'stereo' fibers.~~ The AFE boards connected to the Central Preshower fibers, in addition to using different coupling capacitances, must also have different logic to electrically recombine the North and South halves to form only <u>one</u> discriminator bit for the two halves, while still treating the halves separately in the A/D conversion.[1] The remaining 'stereo' fibers are handled by other AFEs that connect directly to DFE boards. A simple block diagram of this arrangement is shown in Figure 1.

[1] The OR function of the Preshower was a feature of the 12-MCM boards and was not a requirement of the 8-MCM boards. Fortunately, the 8-MCM design incorporated extra traces in the printed circuit board against the possibility that the detector might be miswired, and this fatalistic foresight turned out to be exactly the solution to the OR function problem.

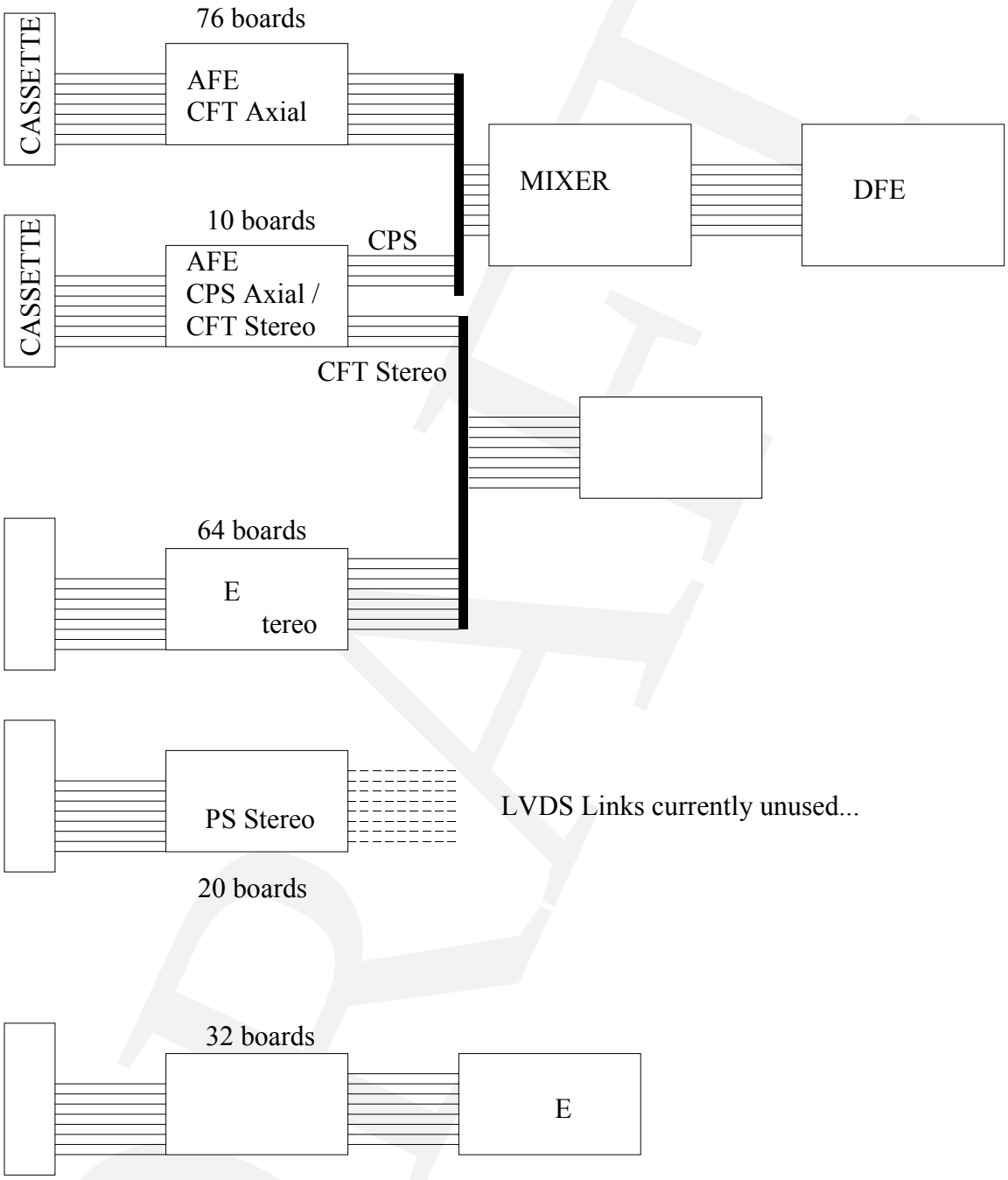

Figure 1

A more detailed picture of the actual routing of the discriminator data wiring between the AFEs and the Mixer/DFE (CFT Axial) in Figure 2 shows some of the trouble caused by the change in detector fiber connections alluded to earlier. The reader is requested to note the rather complicated wiring scheme connecting AFE to Mixer, especially compared to the original scheme in which there was no Mixer and all the runs from AFE to DFE were straight lines.[2]

[2] Many thanks to Jamieson Olsen for picture used as Figure 2.

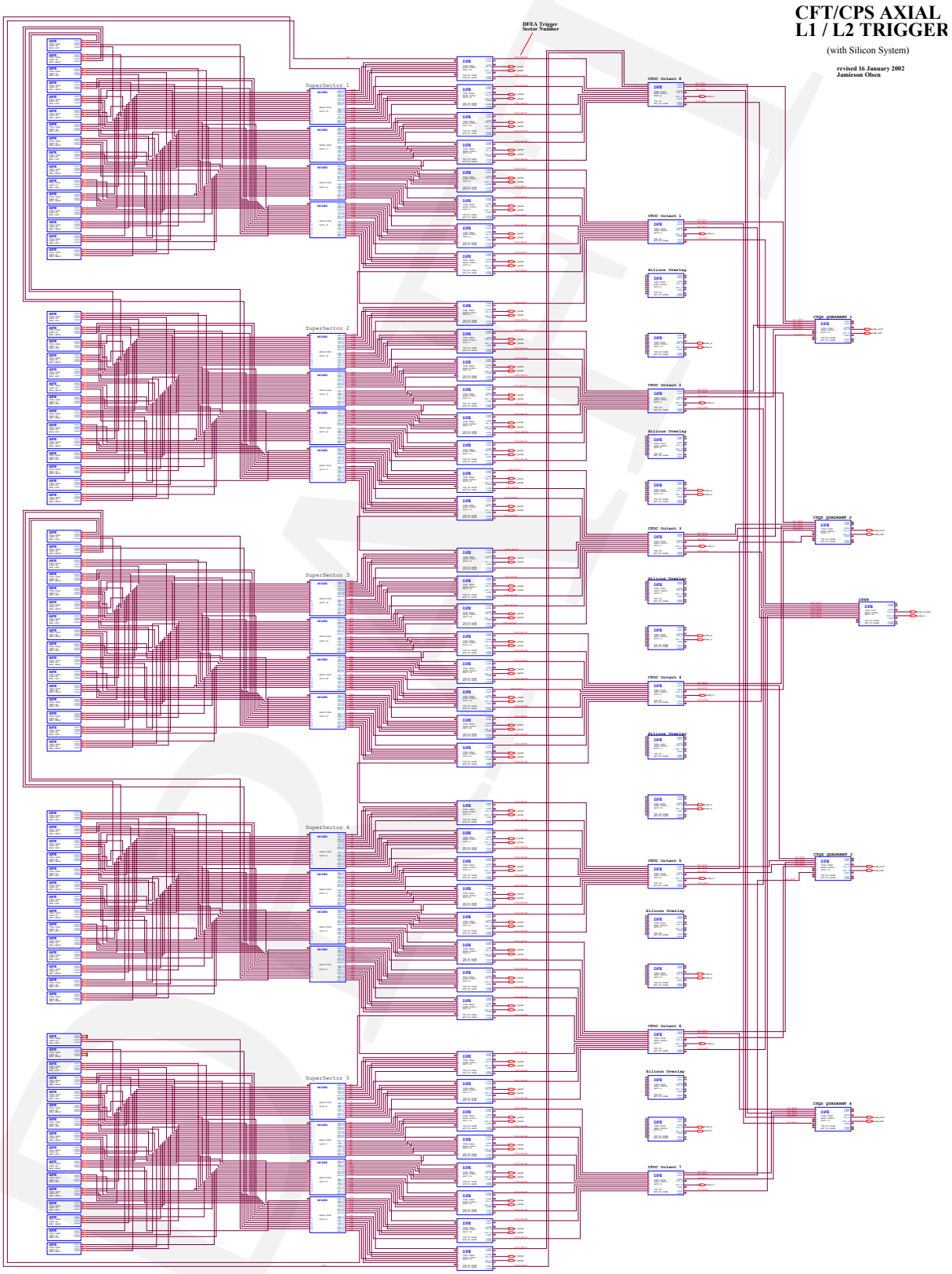
CFT/CPS AXIAL
L1 / L2 TRIGGER
(with Silicon System)
revised 16 January 2002
Jamieson Olsen
DFEA Trigger
Sector Number
SuperSector 1
SuperSector 2
SuperSector 3
SuperSector 4
SuperSector 5
CTOC Octant 0
CTOC Octant 1
CTOC Octant 2
CTOC Octant 3
CTOC Octant 4
CTOC Octant 5
CTOC Octant 6
CTOC Octant 7
Silicon Overlay
CTOC QUADRANT 1
CTOC QUADRANT 2
CTOC QUADRANT 3
CTOC QUADRANT 4
CTOT

Figure 2

For further details of the detector arrangement, please access the detector pages on the web. A reasonable starting point is
http://D0server1/Projects/TriggerElectronics/WebDocs/Trigger_index.htm

~~For the purposes of this document, it is sufficient to note that all the fibers from the detector are landed into either 8-MCM or 12-MCM boards, and that all 512 channels of the 8-MCM AFE are single-threshold. In the 12-MCM variation, 256 channels are single threshold while the other 256 are dual-threshold.~~

All channels of analog data seen by the AFE boards pass through discriminators. Each discriminator creates one bit of data per input channel, creating a bitmap of fibers whose charge was above threshold. This pattern is sent to Digital Front End (DFE) boards every crossing of the beam (every 132 nsec) by high-speed serial data links. The AFE was designed for use at 132 nsec beam crossings; in 396 nsec accelerator operation the data transmitted one of every three crossings contains the discriminator information plus system timing bits and the other two contain only the timing bits with zeroes where the discriminator data would be. There is a single DFE for each of the 80 detector sectors; each takes the discriminator bit pattern for an entire sector and uses FPGAs to match possible track roads to the bit pattern. To obtain sufficient bandwidth for 132 nsec operation, each 8-MCM AFE board must drive four parallel gigabit digital links (512 bits every 132nsec = 3.878 Gbit/sec).

The DFE boards feed the trigger processor logic. When the trigger system declares a Level 1 Accept, the SVX Sequencer boards cause the SVX chips in the AFEs to digitize the charge held in the SVX analog pipeline for every channel.. The AFE sends all the SVX data, plus a redundant copy of the discriminator bits that were previously sent that caused the trigger (buffered in the Virtual SVX logic), as a data stream to the SVX Sequencers for inclusion in Level 2 trigger processing. Upon completion of SVX readout the AFEs return to sending discriminator data.

Conversion of the photon signal from the CFT fibers into a charge signal is accomplished using cryogenic Visible Light Photon Counter (VLPC) photodetectors. The charge signals from the VLPCs connect directly to the AFE.

1.3. Description Of Component & How It Fits Into The System

The 8-MCM AFE board is a multilayer printed circuit board which is 9U (14.435 inches) high and 19.25 inches deep. Each AFE slides into guide rails in a mechanical cassette which houses the light-to-charge conversion circuitry. As the AFE is installed into the cassette, it plugs into a backplane from which it derives power and control connections. After insertion into the cassette, a set of flexible circuit cables is connected to the AFE along the bottom edge to deliver the analog input signals.

The cassette is a complex mechanical assembly. One AFE is mounted on each side of the cassette. Each AFE has its components on the outside, so the AFE must be mirror-imageable left to right so that it may be plugged into either side of the cassette. The cassette electronics requires operation at cryogenic temperatures, so relatively long and specially designed cables bring the low-level analog signals from the bottom of the cassette (held at about 9 Kelvin) to the room-temperature AFE.

1.4. List Of Component Requirements

- Mirror-image left to right design
- Mechanically compliant with cassette design
- Must accept 512 low-level charge signal inputs (typical signal 10fCoul)
- Must discriminate all 512 channels every 132 nsec
- Must deliver digital result of all 512 channels to DFE boards and/or Mixer System every 132 nsec via multiple high-speed LVDS links
- Relatively low power (~40 Watts) due to limited airflow
- Controlled by MIL-STD 1553 interface
- Able to provide test pattern data in lieu of real data
- Interfaces to SVX Sequencers for readout of ~~SVX chips~~ A/D converters using data format identical to that of SVX IIb chips when discriminator pattern is indicative of interesting event
- Buffers all discriminator data for redundant readout of discriminator pattern that caused trigger over SVX bus when ~~SVX~~ A/D chips read out
- Able to act as closed-loop temperature controller for cryostat photoelectronics
- Provide all required clocks to control ~~SIFT~~ discriminator chips

2. THEORY OF OPERATION AND OPERATING MODES

2.1. Basic Features & Operation

The 8-MCM AFE contains a number of subsystems. Figure 3, on the next page, gives the overview. The essential subsystems are as follows:

- Interface to MIL-STD 1553
- Dual-port RAM between 1553 interface and internal microprocessor
- Microprocessor with built-in A/D converter
- ~~DAC system to develop all control voltages for SIFT chips in the MCMs~~
- A clock generation system to develop all required timing clocks for the ~~SIFT~~ TRiP chips
- Eight ~~Multi-Chip Modules (MCMs)~~ analog conversion sections that perform measurment of the analog signals
- A 'Virtual SVX' (VSVX) system to buffer discriminator data for readout with ~~SVX data~~ the A/D data from the analog conversion sections
- An interface to the SVX Sequencer for control and readout
- Analog monitoring, closed loop temperature control system and bias voltage control for the VLPCs
- High speed data multiplexing system which takes all discriminator data from the SIFT chips and sends it via LVDS links to the DFEs.

~~The heart of the AFE is eight Multi-Chip Modules (MCMs) which each contain four SIFT discriminator chips and one SVX II charge-sensitive ADC. Each MCM can 'see' up to 72 channels of charge input. Every 132 nsec the SIFTs provide one bit of discriminator output per channel, where a '1' indicates that the charge delivered to the SIFT was above a threshold set by a control voltage. The charge collected by each channel of each SIFT is transferred using a switched-capacitor charge pump to an SVX II chip such that the entire event is stored in the analog pipeline of the SVX. Should the discriminator pattern of this and all other trigger AFE boards indicate an interesting event, the Level 1 Trigger initiates a readout of the SVX II chips in all the AFEs, which provide 8-bit digitization of the stored charges, analog readout of the same charge pattern that caused the trigger in the first place.~~

The middle of the AFE contains eight analog subsections, each containing two TRiP discriminators, two commercial A/D converters and control logic. Each TRiP has 32 channels of charge input. Every 132 nsec the TriPs provide one bit of discriminator output per channel, indicative of whether the charge delivered to the TRiP was above a threshold. The charge collected by each channel of each TRiP is also held in an analog pipeline. Should the discriminator pattern of this and all other trigger AFE boards indicate an interesting event, the Level 1 Trigger initiates a conversion and readout of the A/D chips in all the AFEs, which provide 8-bit digitization of the stored charges, analog readout of the same charge pattern that caused the trigger in the first place.

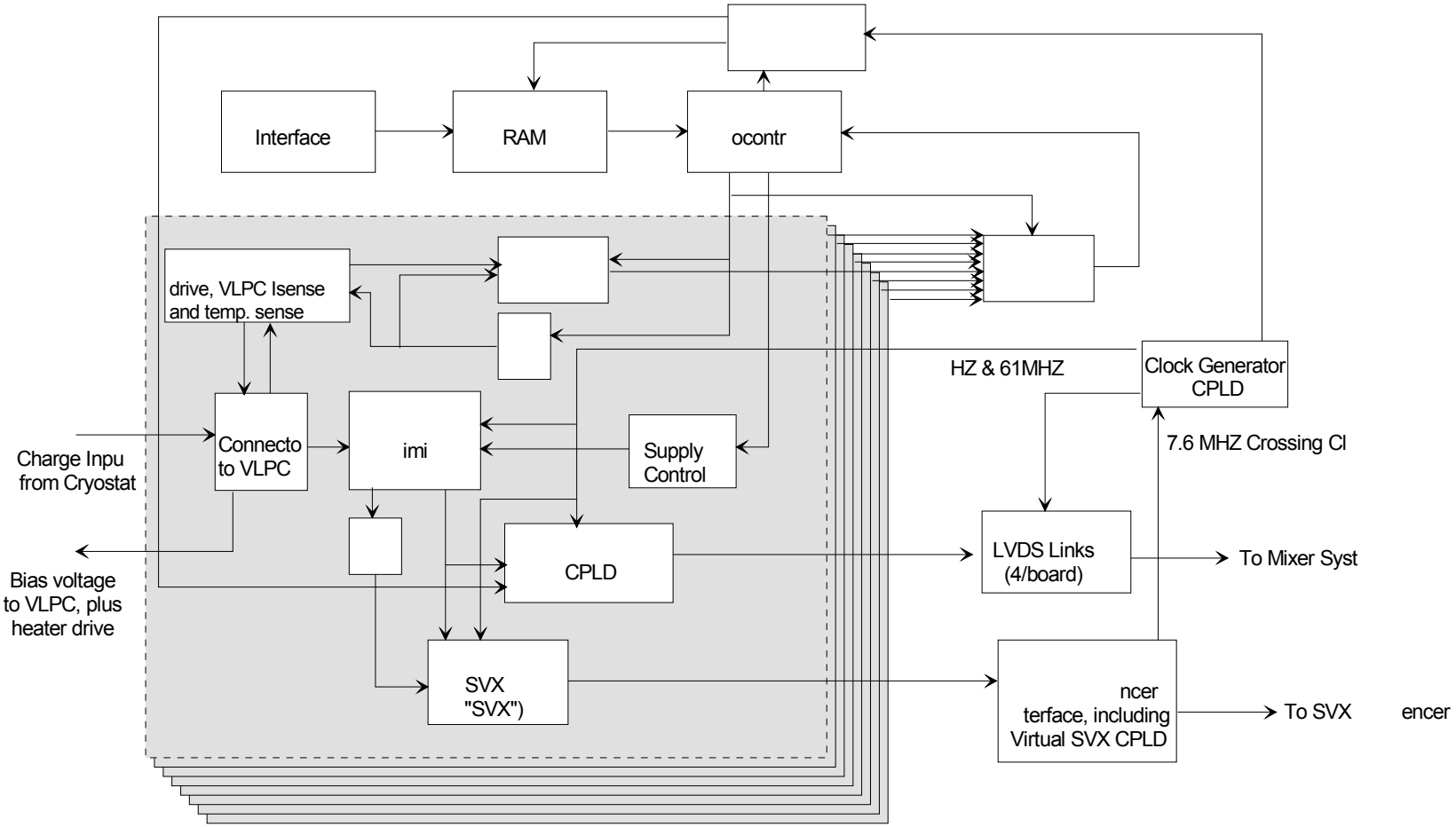
Interface
RAM
ocontr
drive, VLPC Isense
and temp. sense
HZ & 61MHZ
Clock Generator
CPLD
Connecto
to VLPC
imi
Supply
Control
7.6 MHZ Crossing Cl
Charge Inpu
from Cryostat
CPLD
LVDS Links
(4/board)
To Mixer Syst
Bias voltage
to VLPC, plus
heater drive
SVX
"SVX")
ncer
terface, including
Virtual SVX CPLD
To SVX
encer

Figure 3

2.2. Diagnostic Features

Numerous diagnostics are built into the AFE:

- The microprocessor can read back all the DAC settings associated with cryostat control and verify the DACs are working.
- The microprocessor can perform local RAM diagnostics.
- ~~The microprocessor can 'snoop' on SVX data readout and/or insert test data into the SVX data readout; this also allows redundant readback of SVX and VSVX data over the 1553 bus~~ [3]
- The MIL-STD 1553 interface provides read/write loopback capability for testing the interface from the remote computer
- All major logic functions are provided using in-system programmable logic devices.
- The CPLDs which read out the ~~SIFT~~ TRiP chips can insert test patterns into the LVDS readout to the Digital Boards, including a 'fake track' pattern that can be used to test the Mixer/DFE connection downstream.
- The Virtual SVX logic can insert test patterns in place of discriminator data and isolate itself from the rest of the readout for diagnosis of token passing failures.
- Cryostat temperature, board voltages, board temperature and other analog parameters can be continually monitored by the microprocessor and reported to online systems via the 1553 interface.

2.3. MIL-STD 1553 Interface

The MIL-STD 1553 serial link is used as the main control connection to the AFE board. Each AFE has its own Remote Terminal (RT) interface which implements the required timing. To the 1553 system, each AFE implements three subaddresses, 16, 17 and 18 (0x10, 0x11 and 0x12). Each board appears to be a ~~2K X 16~~ 64K X 16 RAM[4] where subaddress 16 is the address in the RAM where data is read/written, and subaddress 17 is the port where the data is read or written. Subaddress 18 is reserved for bench diagnostics and is not normally used.

A few locations in the RAM are reserved as a 'command queue' which is loaded by the 1553 controller with eight-bit command values. The queue is filled with commands and, when the list is ready, a terminal value is written to a different address which causes the on-board microprocessor to implement the list of commands previously stored. The rest of the RAM is allocated to status information, command arguments and board settings. All RAM locations are available to the 1553 interface, which may interrogate them at any time.

[3] Although implemented and proven to work on AFE I, this feature was never used outside of the test bench and shall be deleted in AFE II to save cost.

[4] The excess storage capability of the dual-port RAM is used solely for downloading programming information to the FPGAs that will be on the AFE II. All addresses and features used by experiment control programs shall remain at the same addresses as in the AFE I, preserving backwards compatibility.

All commands and their interpretation are controlled by the firmware of the on-board microprocessor, which is EPROM based and thus cannot be trivially changed by the end user. Engineering note A1000612, at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a1001612.pdf

provides a detailed look at the memory map of the board. The 1553 interface of the AFE is compatible with the VME-to-1553 interface used elsewhere in D-Zero, originally designed by the Accelerator Division Controls group. This board is found in both the detector and at all AFE test stands. The necessary software information to use this VME interface to 1553 may be found at http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990312a.pdf

2.4. Dual-Ported RAM

All accesses to the AFE from the 1553 bus load data into or read data from a dual-ported ~~2K X 16~~ 64K X 16 synchronous RAM. Since the internal microprocessor uses an eight-bit bus, the RAM on the microprocessor side is organized as ~~4K X 8~~ 128K X 8. The dual-port architecture allows this bus width change and also allows simultaneous access from both sides, simplifying any collision detection. ~~The microprocessor side of the RAM is subservient to the 1553 side, such that if the micro tries to access the same location as is currently addressed by 1553, the micro will receive a BUSY signal and must wait it's turn~~. The synchronous architecture of the RAM is used to avoid collisions by time-slicing the 1553 and microprocessor access. The RAM cycle time is small compared to the access rate of either side and so a pair of non-overlapping clocks allow both sides non-contentious access.

Any 16-bit value written to the DPRAM by the 1553 interface is presented to the micro as two bytes at adjacent addresses; however, since there are twice as many microprocessor addresses, the address from the micro side is double the address from the 1553 side Thus, the 16-bit address 0x35 from the 1553 side is the same data as the two bytes at addresses 0x6A and 0x6B from the microprocessor side. The current addressing convention is that the even address from the micro side is bits 7:0 of the data from the 1553 side, and the odd address is bits 15:8.

2.5. Flash RAM

A Flash RAM chip has been added to the design of the AFE II as support for FPGA chips that are now part of the analog conversion circuits and replace some of the CPLD logic of the original design. The use of FPGAs is simply based on cost. Replacement of the SVX chips by commercial A/D parts necessitates addition of another set of FIFOs to the board. With sufficiently cheap bulk code storage, an FPGA embedding two FIFOs and replacing one of the CPLDs originally used to control the original FIFO is the most cost-effective solution. The most cost-effective bulk storage for the FPGA program is Flash RAM.

The Flash RAM is connected to the same address and data bus as the dual-port RAM described above. An additional address latch expands the available address bus from 16 bits to 24 bits, and a couple of extra decodes derived from the Helper CPLD provide access to the Flash. The microprocessor code will be changed such that upon power-up or command the contents of the Flash are downloaded to the FPGAs. Sector erase and sector program commands shall also be added, utilizing the new large buffer available in the expanded DPRAM to hold one sector of data.

The FPGA currently planned for the AFE II is the Xilinx XC2S30, which requires about 300,000 bits of configuration data per FPGA. Eight of these FPGAs (one per analog block) are expected. Allowing for the usual feature creep, 128 kBytes of Flash (two sectors) is allocated for each FPGA, enough to allow expansion to the XC2S50. End users will inevitably demand the capability to download FPGA code via the 1553 interface and reprogram the FPGAs on boards installed on the detector. To insure reliable detector operation, enough Flash must be implemented to allow for two downloads of each of eight FPGAs (one set of downloads for users to play with and one set they can't write to as the known-working backup). At two sectors per FPGA, 2 downloads * 8 FPGAs * 2 sectors/FPGA = 32 sectors of 64 kbytes each are thus required. A 16 Mbit Flash will suffice, and is *far* less expensive than PROM.

2.6. Microprocessor

A Microchip PIC 14000 microcontroller is used on the AFE. The PIC 14000 is chosen because it combines a sufficiently large code space (4K words), internal A/D converter, reasonable clock speed and integrated I^2C bus support into one package. The microprocessor provides supervisory and diagnostic control functions in the AFE but in no way interferes with the high-speed data acquisition functionality. The basic jobs handled by the micro are the following:

- Poll the dual-port RAM and respond to commands from the 1553 bus;
- Load analog control voltages to the DAC subsystem over the I^2C bus;
- Perform analog readback of DAC voltages, board temperature, board power supply voltages and cryostat temperature using its internal A/D converter;
- Sequence the power supply turn-on and turn-off to the ~~SVX and SIFT~~ TRiPchips;
- Act as local closed-loop temperature controller for the VLPC chips in the cassette.

The microprocessor firmware is coded entirely in assembly language and is not available to the end user once installed in the AFE. The chip itself is EPROM-based which allows changes to the firmware, but only if access to the AFE board itself is possible. Remote downloads of firmware are not supported.

A 'helper' CPLD demultiplexes the microprocessor I/O lines and provides the necessary support to address the dual-port ram, and write/read the various internal registers of the board. Most internal registers are not made directly accessible to the end user but instead are manipulated in fixed fashion in response to command codes sent to the micro by the end user. This insures that only known working sequences of register operations ever occur.

The microprocessor clock is derived from the on-board 1553 interface clock, so that the micro will run even if the AFE is disconnected from the rest of the fiber tracker system.

2.7. DAC Subsystem

~~Each of the eight multi-chip modules (MCMs) in the AFE require numerous analog control voltages to function:~~

- ~~For each of the four SIFT discriminator chips within the MCM (each SIFT handles 18 of the 72 channels within the MCM), there is a threshold voltage which determines the required charge for the discriminator to yield a '1'. Due to vagaries in the SIFT design the threshold is actually the difference between two voltages that have a common-mode point of 2.5 volts; this, however, is hidden from the user by the use of a couple of op-amps that derive the companion voltage from the DAC setting.~~
- ~~For each of the four SIFT discriminator chips within the MCM there is also a reference voltage V_{REF} which controls the pedestal and dynamic range of the charge transfer from the SIFT to the SVX II chip used as the 8-bit A/D of the AFE.~~
- ~~Each pair of SIFT chips also requires a dynamic range control voltage.~~
- ~~There is also a charge transfer circuit clamp voltage V_{CLMP}, common to all four SIFTs in the MCM.~~

~~The dynamic range control and V_{CLMP} voltages may be supplied by simple resistor voltage dividers, but the other eight voltages must be variable. Thus, each MCM has associated with it an octal DAC. The nominal gain of the SIFT is about 30 fCoul per volt, with a maximum range of about 150 fCoul. Thus, with an eight-bit DAC, the threshold can be ideally set in 0.585 fCoul steps. However, offset differences between the SIFTs and noise will probably limit the resolution to 1-2 fCoul.~~

~~In addition to the eight octal DACs required to provide all of the MCM control voltages,~~ Each of the eight input cables from the cryostat to the AFE have some analog voltages associated with them:

- A bias voltage supply for the VLPC photodiodes;
- A constant current supply for the temperature sense resistor;
- A heater drive supply for the temperature maintenance resistor mounted adjacent to the VLPCs in the cryostat.

Two channels of DAC are assigned for each cable, one for the bias voltage and one for the heater supply. The constant current supply is fixed. Two octal DACs thus suffice for all eight cables~~, for a total of ten octal DACs (eighty DAC channels) across the board~~. A single I^2C bus allows the microprocessor to control both DACs and the analog muxes used for loop feedback. A third DAC is added to the AFE II board to provide a 'VCAL' calibration voltage for the TRiP chips in place of the VCAL supplied by the Sequencer, which is both noisy and too large a voltage range. A single octal DAC provides a uniquely programmable voltage per TRiP. Provision for connection of this multiplying DAC to a sinusoidal source for DNL testing of the TRiP in-place is also made.

~~The I^2C bus addressing mechanism for the octal DAC parts allows for only four octal DACs on the bus, so a bus switching scheme is implemented that partitions the board into four~~

~~I^2C sub-buses. Sub-buses 'A' and 'B' are used to control the eight MCMs, and sub-bus 'D' controls the cable voltages. Sub-bus 'C' is reserved for address expansion as will be required on the 12-MCM variant of the board. Further details of the DAC subsystem design may be found at~~

~~http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990607a.pdf~~

~~This document is also undergoing some revision but is reasonably up to date.~~

2.8. Clock Generation

The AFE board must synchronize to the 7.6 MHz beam crossing clock as provided by the SVX Sequencer boards in order to correctly acquire the data. However, in order to transmit the data to the Digital Boards, a faster clock is required. A phase-locked loop is used to multiply the beam crossing clock by 7 to generate 53.104 MHz, the usual RF clock frequency found in Fermilab applications. This clock is used as the data clock to the LVDS serial links which transmit the discriminator data from the SIFT chips to the Digital Boards.

A second PLL is used to multiply the beam crossing clock by eight to create the data rate clock for the Virtual SVX subsystem. Since the ~~MCM~~ TRiP has a total of 64 channels and the Virtual SVX must be read out using the byte-wide SVX data bus, this faster clock is required in order to pack all the discriminator bits up into bytes and keep up with the crossing rate.

The Clock Generator also uses silicon delay lines and CPLD logic to create all of the various clock signals required by the SIFT for operation. The crossing clock is sent through the delay lines and the leading edge of each delay tap is used to set and reset asynchronous latches in the CPLD, creating SIFT control clocks with 5nsec edge placement relative to each other and to the crossing clock. Various programs in the CPLD may be loaded to compensate for slight differences in fiber length and/or SVX Sequencer delays, insuring that the SIFT acquisition interval is properly timed with respect to the time when charge is delivered.

A more detailed analysis of the clock generator may be found at

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990105a.pdf

~~2.9. Multi-Chip Modules~~ TRiP Discriminators

~~The Multi-Chip Modules contain four SIFT custom ASICs which function as 18-channel discriminators and charge transfer switches. Each SIFT has an individual charge threshold setting. The timing clocks are common among all four SIFTs. When the charge is collected by the SIFTs the discriminator measurement is made when the Sample-and-Hold (S/H) switch is closed. An internal RC network and high-impedance buffer insure that the S/H result persists during the next crossing interval, allowing plenty of time for the CPLDs to latch the data. This same S/H signal also causes the charge to be copied – at a less than unity gain – onto a holding capacitor. A subsequent READ clock transfers the charge from all four SIFTs to an SVX IIe chip inside the MCM, which acts as a 128-channel, 8-bit charge sensitive ADC.~~

The TRiP is a 32-channel device combining a 48-level deep analog pipeline with a discriminator. ~~The SVX IIe implements an analog buffer such that charges collected from the SIFTs are held for up to 31 crossings until discarded.~~ Should a trigger accept occur within the 48 crossings, the Sequencer will cycle through Digitize and Readout modes, during which the charge stored in one of the pipeline capacitors is digitized by the external A/D converters and read out through the FPGAs to the Sequencer. ~~SVX IIe may then be placed into the Digitize and Readout modes in order to perform the actual A/D conversion~~. Since conversion occurs only

upon demand, new charge may be placed into the chip every crossing until a conversion is required. The discriminator outputs run continuously and are not buffered within the chip. Every live beam crossing the discriminator outputs are latched and sent to the Mixer subsystem through a time-multiplexing CPLD and an LVDS gigabit serial link.

~~Each MCM is a large, 228 pin surface mount device which contains the five ASICs plus numerous resistors and capacitors on a high density printed circuit substrate. Each MCM is individually tested on a separate MCM Test Board prior to their being soldered onto the AFE boards. Precious little up-to-date information on the SIFT is available on the Web; contact the author for paper copies of documentation and/or SPICE models. The MCM itself was designed by Mike Matulik (matulik@fnal.gov) .~~

2.10. Virtual SVX Subsystem

The Virtual SVX subsystem utilizes a set of CPLDs which capture the discriminator data ~~from the MCMs~~ and buffer this data into small Event Delay FIFOs. These FIFOs provide the same amount of digital buffer depth as is provided by the analog buffer in the ~~SVX IIe~~ TRiP chip, such that when a trigger occurs, the discriminator pattern which caused the trigger may be read out in addition to the ~~SVX IIe~~ TRiP data of the event. The intent of this is to provide calibration information where the ~~SVX IIe~~ TRiP values can be compared against the SIFT discriminators, providing a cross-check of discriminator thresholds.

Each ~~MCM~~64-channel input group has a 512 X 8 FIFO, called the Event Delay FIFO, associated with it to handle this delay function. A ~~CPLD~~FPGA with an internal 512 X 8 FIFO monitors the state of the ~~SVX IIe~~ TRiP chips. During normal acquisition, this ~~CPLD~~ FPGA counts clocks, and when the FIFO buffer depth is equal to the delay that's been programmed into the ~~SVX IIe~~ TRiP chips, it then maintains the FIFO depth at that point by issuing read clocks and discarding the data at the same rate that new data is put into the FIFOs. This insures that at all times the data at the outputs of the FIFOs is the digital data of interest. When the level 1 trigger accept signal is received, the ~~SVX IIe~~ TRiP chips enter a Digitize mode. During that same time interval the VSVX CPLD collects all the data from the eight Event Delay FIFOs and prepares the data for readout. After the Digitize cycle is complete the ~~SVX IIe~~ FPGAs, which contains all the digitized charge information from the TRiP chips, are read out. A token is passed from chip to chip (i.e. from FPGA to FPGA). When the token falls out of the last FPGA, it goes to the Virtual SVX, which then reads out the discriminator data in a format compatible with the SVX IIe data format expected by the Sequencer.[5]

A detailed analysis of the Virtual SVX system is available at

[5] A proposal has been made to pack the discriminator bit for each channel into the address byte for each channel (with 64 channels, only 6 bits are required, leaving the 7th bit as the discriminator bit), and eliminate the VSVX as a separate potion of the data stream. While technically possible, at present this is not planned to be implemented for two reasons:

1) This violates the 'plug-in replacement' rule, as the data format would be different.

2) Channels below the zero suppression threshold ADC value, but still have the discriminator bit set (an error condition), would be undetected in the compressed format.

None the less, the hardware implementation shall include sufficient extra traces to allow for the possible implementation of the compressed format at some future time.

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a991015a.pdf

2.11. SVX Sequencer Interface

The SVX Sequencer is an external circuit board mounted in a rack near the AFE boards. A ribbon cable connection from the SVX Sequencer to the AFE provides a bidirectional data bus, required control signals and clocks. Some of the control bits (timing markers such as Sync Gap or L1_Accept) are used by the AFE; all are passed through the board into the LVDS data stream for use in the Mixer and/or DFE boards. The Sync Gap is used by the AFE as the main timing marker to resynchronize the internal counters that mark the 'live' and 'dead' crossings in the 396 nsec mode of operation. The SVX Sequencer is the source of the master clock (7.6 MHz) which all discriminator timing is derived. The Level 1 Accept (the master trigger signal which initiates readout of the ~~SVX IIe~~ TRiP chips and the Virtual SVX) is also carried over this cable. The cable as currently implemented contains a number of SVX-specific characteristics and signals which are not well matched to the AFE II. Specific consideration must be given to the following situations:

- The SVX has four modes of operation (Initialize, Acquire, Digitize and Readout). While the latter three are well matched to TRiP functions, the Initialize mode is not so well matched. The TRiP initialization string is significantly different in length and format as compared to the SVX string. The code controlling the Sequencer will have to be modified (violating the no-external-difference rule) unless an alternate, additional path through the dual-port RAM, 1553 interface and microprocessor is implemented.
- The AFE I – to – Sequencer link suffered bandwidth limitation (maximum readout clock of 40 MHz) due to poor delivered 53 MHz clock quality from the Sequencer. AFE II will address this by using the on-board 53 MHz clock as the readout clock. Tests of a modified AFE I board show that this approach can even work with the SVX/MCM combination to decrease experiment deadtime.[6]

The SVX Sequencer was designed by Mike Utes and documentation for this module may be found at

http://d0server1.fnal.gov/users/utes/default.htm

[6] A relatively simple modification to the AFE I board allows this board to read out at 53 MHz instead of 40 MHz. A jumper is removed, two short (< 2 inch) green wires are added and one CPLD is reprogrammed so that the internally generated 53 MHz clock is used as the Readout clock, not the clock given to the board by the Sequencer. One of the Sequencer CPLDs must also be reprogrammed to match. While the AFE part of the modification is transparent – it allows external selection of readout speed – the Sequencer portion is not. The Sequencer uses CPLD logic cell delays to 'tune' the delay of DVALID relative to the data and the particular CPLD performing this function has no interface to VME. Because of the non-transparent nature of the modification, the deadtime improvement has been deferred until a sufficiently long access is granted to allow modification and testing of a large group of AFE & Sequencer boards.

2.12. Analog Monitoring and Control

Various analog control circuits interface to the microprocessor in order to control the system. ~~A couple of op-amps are used with each MCM in order to generate the mirror-image voltage of the threshold setting, as the SIFT threshold voltage is defined as the difference between two voltages centered about 2.5V, not a simple voltage with respect to the main return.~~ A pair of op-amps per VLPC cable are used to create the constant current used to measure the temperature of the VLPC. A carbon composition resistor is used which is on the edge of superconductivity at the normal operating temperature of about 9 Kelvin. The voltage dropped across this resistor is measured using an instrumentation amplifier and this voltage is sensed by the A/D converter of the microprocessor through an analog multiplexer. In similar vein, a power op-amp is used to drive a heater resistor should the VLPCs be too cold. Since the normal temperature of liquid helium is about 4.3 Kelvin, the heater resistor is expected to be used regularly. A bias voltage is also required for the VLPCs themselves, and this is driven by an op-amp from a DAC output. The voltage applied to the VLPCs is brought back to the microprocessor A/D, as is a measurement of the current being drawn by the VLPCs.

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990607a.pdf provides a more detailed analysis of this subsystem, and of how the VLPC temperature is maintained.

2.13. Data Multiplexing and Serial Links

The 512 bits of discriminator data obtained every 132 nsec must be transmitted a few feet to the Mixer System (or, for other fibers, directly to Digital Boards). Obviously, a massively parallel cable would be most impractical. To accomplish this transfer, a dual serialization scheme is employed. At each of the eight analog circuit blocks a CPLD takes the 64 bits of discriminator data and, using the 53 MHz clock, creates seven 10-bit words every 132 nsec. The extra six bits are filled with timing signals from the SVX Sequencer.

These eight 10-bit buses are combined in pairs to form four 20-bit buses. Each 20-bit bus is connected to an LVDS driver part which internally multiplies the 53 MHz clock by another factor of seven. The driver part takes a 21-bit input at 53 MHz and sends it out as three data bits (plus a sync clock) at a rate of about 371 MHz. Thus, each 128 bits of MCM data are transmitted over four differential pairs at this 371 MHz rate. Four of these high-speed serial links are then capable of transmitting all 512 bits of MCM data, plus 48 bits of other information, every 132 nsec. The Sequencer bits are transmitted redundantly as they are important control bits for both the Mixer and DFE systems.

The 21st bit of each link is connected to the 7.6 MHz crossing clock so that each Mixer board may check synchronization between all links presented to that board. Since the data to the LVDS drivers is presented at 53MHz, the crossing clock should result in this bit being set one word out of every seven. For those interested in how the LVDS part works, the data sheet is available at

http://d0server1.fnal.gov/projects/triggerelectronics/procurement/cft%20axial/data%20sheets/SN65LVDS95.pdf

3. EMBEDDED & DIAGNOSTIC/DEVELOPMENT SOFTWARE

The AFE board utilizes embedded software in the on-board microprocessor to respond to commands from the external world that appear on the MIL-STD 1553 bus. Diagnostic software uses the embedded routines to gain access to the various features of the board. Diagnostic software has no direct control over the board; everything has to go through the microprocessor.

3.1. Embedded Software

All embedded software in the AFE microprocessor is written in assembly language. The PIC 14000 has a very simple language structure consisting of fewer than 40 mnemonics. The datasheet for the device is located at

http://d0server1.fnal.gov/projects/triggerelectronics/procurement/cft%20axial/data%20sheets/pic14000.pdf

which contains a complete description of the instruction set in Chapter 11.

3.1.1. Software Tools & Methodologies

The standard MPLAB assembler for Microchip PIC products is used. This assembler is available free of charge from Microchip at http://www.microchip.com. The source code for the PIC14000 is found on the D0 server at

http://d0server1.fnal.gov/projects/triggerelectronics/cae/afe_test_module/firmware/20020214/*.asm

Following modular program structure, numerous files are used to build the program. The MAINPROG.ASM file contains the main program and initialization routines. The CMDPROC.ASM file shows the jump table for handling the various commands, and board hardware related constants are held in HDECODE.ASM. All other files handle particular I/O chores and/or the temperature control code.

3.1.2. Description Of Embedded Software

The basic structure of the program is to initialize the ports of the microprocessor and then enter a polling loop where commands from the MIL-STD 1553 interface are handled. A jump table is implemented which provides access to various command handling routines based upon the eight-bit command code sent to the processor, as shown in this code fragment:

```
CMD0        GOTO POLL_CMD       ;since we require the commands to be non-zero,
;                                this is merely a placeholder.
;                                A command of zero exits the processing loop
;                                by going back to the poll routine.
CMD1        GOTO TEST_Q         ;create internal test charges using CREF & TREF
CMD2        GOTO SET_EVENT_DELAY      ;get data from user and sends to register
CMD3        GOTO NULL_CMD
CMD4        GOTO NULL_CMD
CMD5        GOTO TURNON_PS            ;command 5: turn on power supplies
CMD6        GOTO TURNOFF_PS           ;command 6: turn off the power supplies
CMD7        GOTO NULL_CMD
CMD8        GOTO NULL_CMD
```

```
CMD9          GOTO NULL_CMD

CMDA          GOTO UPDATE_AtoD    ;command a: read data from A/D converter, store in
DPRAM (disabled)

CMDB          GOTO NULL_CMD

CMDC          GOTO SET_DIG_CTL    ;command c: write control value to digital control
latch

CMDD          GOTO NULL_CMD

CMDE          GOTO NULL_CMD

CMDF          GOTO UPDATE_DAC           ;command f: copy data values from DPRAM to DAC
```

The number of commands which the microprocessor can support is limited only by the fixed code space of the microprocessor. The reader is reminded that the microprocessor code space is limited to the 4K words within the device itself; no expansion of program memory is possible by the addition of more RAM to the board. The code space of the processor is implemented as two 'pages'. Page 0 is used for all the generic support and for all command processing. Page 1 is used for the temperature control loop.

No interrupts are used in the code to insure stability of operation. The main loop is a simple polling loop that looks for either a command to be present (by reading the DPRAM) or for a timer to expire (indicative of the need to perform a temperature control update). The poll rate is far in excess of either the maximum 1553 command rate or the temperature control speed, so no real-time concern exists here. Some commands can take significant amounts of time to elapse, and so a backup hardware real-time clock has been implemented in a PLD so that the temperature control loop can check to see if its timing counter has "lost" a few ticks during long commands.

The temperature control methodology is a straightforward PI loop. No D term is used and tests have shown it unnecessary. The integration is performed using summing and averaging. The external software sets a desired setpoint for each VLPC block (64 channels) and each of the eight VLPC blocks is independently controlled. Data from platform running to date indicate that the VLPC temperature is maintained to no worse than ±50mK, and in many cases approaches ±10mK. Stefan Gruenendahl need be commended for the significant amount of effort he put in writing and testing temperature control code.

3.2. Development & Diagnostic Software

Diagnostics for the AFE board are provided using a PC running Microsoft Excel, using underlying Visual Basic for Applications (VBA) code extensions. Bob Angstadt of D0 (angstadt@fnal.gov) has written a DLL which allows PCs to utilize one of the Bit3 interfaces to gain access to an external VME subrack. This VME subrack may then use one of the VME-to-1553 interfaces available at the experiment to control the AFE. Many tests may be performed using a list processor macro designed by Bob. VBA standalone programs have been produced for use at the different test stands which automate the testing procedure to fair degree.

3.3. Description Of Hardware Test Platform

The AFE board is tested using a graded sequence of test stands. Inspection and assembly QA tests comprise phases 1-3 of the test procedure. Following this, three test stands exercise each board:

- The Phase 4, or "repair" stand, exercises all basic functions of the board. At Phase 4, the PLDs are programmed, 1553 communications, Sequencer interfacing, microprocessor operation, discriminator operation and A/D conversion are all checked. A board passes Phase 4 if all control and readout functions work and all channels show analog response; however, Phase 4 cannot inject charge to the inputs and so all testing is done using only noise as input.
- Because of the physical structure of the Phase 4 test stand, the board is highly accessible. The Phase 4 test stand is used for diagnosis and repair of all dysfunctional boards.
- The Phase 5 test stand places the AFE board into one cassette, identical in mechanics to the cassettes of the platform. Charge is injected at Phase 5, using a separate AFE Test Module (AFETM) designed by J. Anderson and M. Matulik. The AFE Test Board uses an array of high-speed surface mount NPN transistors to generate test charge pulses which are fed to the inputs of the AFE over the same cables as are used on the platform, to most closely match parasitic loads. A copy of the same MIL-STD 1553 interface and microprocessor blocks used in the AFE is used on the AFE Test Board to provide a common interface by which the amount of charge delivered to different inputs of the AFE may be programmed. The AFETM includes timing, channel grouping and amplitude controls to allow isolated analysis of channels.
- Phase 5 uses the AFETM to determine the actual analog response of every channel on the AFE and to isolate individual channel problems. The AFETM also emulates the heater/temperature sensing loop of the cryostat so that each AFE may be calibrated. Last, calibration measurements of the delivered bias voltage to each VLPC module are made at this stage.
- Phase 6, also known as the "Combined Test Stand" or "CTS", repeats a few of the basic function tests of Phase 4, but using the SVX Sequencer as the controller and obtaining timing from the accelerator itself. Phases 4 & 5 use the Stand-Alone Sequencer module which generates its own accelerator timing from state machine logic. This test finds any boards with marginal timing.

3.3.1. Description Of Software Test Platform

The Phase 4 software tests perform the usual I/O and RAM tests, followed by sequences in which the various DACs are walked over ranges of values as the board is read out. Phase 4 software checks for valid readouts and/or data errors. Phase 5 software performs a more cursory check of the base functions but does more complex data taking loops with larger data sets for analysis of each individual channel. Phase 6 uses the same software as is used in the experiment control room.

4. INTERFACE SPECIFICATIONS

The AFE board talks to the world through its connection to the AFE Backplane. This backplane provides power, connection to the SVX Sequencer, LVDS output and connection to MIL-STD 1553. Inputs to the board are through flex cables that connect at the bottom edge. The backplane pinout is shown here, as viewed from the back (cabling) side, for a right-handed AFE. The left-handed AFEs have reversed column order.

	F (Top Shield)	E	D	C	B	A	Z (Bottom Shld)
1	GND	5.5V	+3.3V	GND	1553-	1553+	GND(BP)
2	GND	5.5V	+3.3V	GND	SLOTBIT1	SLOTBIT2	GND(BP)
3	GND	5.5V	+3.3V	GND	SLOTBIT8	SLOTBIT3	GND(BP)
4	GND	5.5V	+3.3V	GND	SLOTBIT7	SLOTBIT4	GND(BP)
5	GND	+3.3V	+3.3V	GND	SLOTBIT6	SLOTBIT5	GND(BP)
6	GND	GND	GND	GND	MICRO_STAT 0	MICRO_STAT1	GND(BP)
7	GND	LVDS1_D1+	LVDS1_D1-	GND	LVDS1_D2+	LVDS1_D2-	GND(BP)
8	GND	LVDS1_D0-	LVDS1_D0+	GND	LVDS1_CLK+	LVDS1_CLK-	GND(BP)
9	GND	GND	GND	GND	GND	GND	GND(BP)
10	GND	LVDS2_D1+	LVDS2_D1-	GND	LVDS2_D2+	LVDS2_D2-	GND(BP)
11	GND	LVDS2_D0-	LVDS2_D0+	GND	LVDS2_CLK+	LVDS2_CLK-	GND(BP)
12	GND	GND	GND	GND	GND	GND	GND(BP)
13	GND	LVDS3_D1+	LVDS3_D1-	GND	LVDS3_D2+	LVDS3_D2-	GND(BP)
14	GND	LVDS3_D0-	LVDS3_D0+	GND	LVDS3_CLK+	LVDS3_CLK-	GND(BP)
15	GND	RESVD3+	RESVD3-	GND	LVDS3_D3+	LVDS3_D3-	GND(BP)
16	GND	GND	GND	GND	GND	GND	GND(BP)
17	GND	LVDS4_D1+	LVDS4_D1-	GND	LVDS4_D2+	LVDS4_D2-	GND(BP)
18	GND	LVDS4_D0-	LVDS4_D0+	GND	LVDS4_CLK+	LVDS4_CLK-	GND(BP)
19	GND	RESVD4+	RESVD4-	GND	LVDS4_D3+	LVDS4_D3-	GND(BP)
20	GND	GND	GND	GND	GND	GND	GND(BP)
21	GND	LVDS5_D1+	LVDS5_D1-	GND	LVDS5_D2+	LVDS5_D2-	GND(BP)
22	GND	LVDS5_D0-	LVDS5_D0+	GND	LVDS5_CLK+	LVDS5_CLK-	GND(BP)
23	GND	RESVD5+	RESVD5-	GND	LVDS5_D3+	LVDS5_D3-	GND(BP)
24	GND	GND	GND	GND	GND	GND	GND(BP)
25	GND	+12V	+12V	GND	-12V	-12V	GND(BP)

Table 1 - top half of backplane connector

1	GND	DVALID B	GND	SYNC_GAP	GND	CROSSING*	GND(BP)
2	GND	GND	1st XING	GND	CROSSING	GND	GND(BP)
3	GND	SVX_DAT0 B	GND	VCAL B	GND	PRIORITY_OUT B	GND(BP)
4	GND	GND	DIR B	GND	SVX_DAT2B	GND	GND(BP)
5	GND	SVX_DAT5 B	GND	HDI_EN B	GND	SVX_DAT1B	GND(BP)
6	GND	GND	SVX_DAT3B	GND	SVX_DAT6B	GND	GND(BP)
7	GND	MODE1 B	GND	SVX_DAT7B	GND	SVX_DAT4B	GND(BP)
8	GND	GND	PRIORITY_IN B	GND	CLK* B	GND	GND(BP)
9	GND	CFT_RESET	L1 ACCEPT	CLK B	GND	MODE0 B	GND(BP)
10	GND	CLAMP	GND	SPARE	CHG_MODE B	GND	GND(BP)
11	GND	+5V	+5V	+5V	+5V	+5V	GND(BP)
12							
13							
14							
15	GND	DVALID B	GND	SYNC_GAP	GND	CROSSING*	GND(BP)
16	GND	GND	1st XING	GND	CROSSING	GND	GND(BP)
17	GND	SVX_DAT0 B	GND	VCAL B	GND	PRIORITY_OUT B	GND(BP)
18	GND	GND	DIR B	GND	SVX_DAT2B	GND	GND(BP)
19	GND	SVX_DAT5 B	GND	HDI_EN B	GND	SVX_DAT1B	GND(BP)
20	GND	GND	SVX_DAT3B	GND	SVX_DAT6B	GND	GND(BP)
21	GND	MODE1 B	GND	SVX_DAT7B	GND	SVX_DAT4B	GND(BP)
22	GND	GND	PRIORITY_IN B	GND	CLK* B	GND	GND(BP)
23	GND	CFT_RESET	L1 ACCEPT	CLK B	GND	MODE0 B	GND(BP)
24	GND	CLAMP	GND	SPARE	CHG_MODE B	GND	GND(BP)
25	GND	+5V	+5V	+5V	+5V	+5V	GND(BP)

Table 2 - Bottom half of backplane connector

4.1. MIL-STD 1553 Interface

This interface has been previously discussed. The MIL-STD 1553 interface is a serial protocol carried on two wires, at a bit rate of approximately one bit per microsecond. Manchester encoding is utilized and decoded via a standard interface chip. A CPLD acts as the deserializer and interface to the dual-port RAM.

http://d0server1.fnal.gov/users/janderson/Public_Eng_Notes/a990312a contains a brief description of the 1553 protocol which may be used to understand how this bus works. Numerous other web sites also discuss this bus, which is still in fairly wide use in the avionics industry.

4.1.1. Addressing Modes

The AFE responds only to subaddresses 0x10, 0x11 and 0x12.

4.1.2. Data Cycles Types

Only normal data cycles (no broadcasts) are supported.

4.1.3. Register Descriptions

Subaddress 0x10 is an address pointer register which selects the address of the dual-port RAM which will be read or written by the first access to subaddress 0x11. The dual-port ram has an address range of 0x0000 – 0x1FFF. Any data written to bits 15, 14 or 13 of subaddress 0x10 will be ignored. Having written to subaddress 0x10, reads or writes to subaddress 0x11 access successive locations in the dual-ported memory. The RAM address loaded by the write to subaddress 0x10 is incremented with each data word read or written to subaddress 0x11, such that a 5-word read from subaddress 0x11 after writing a value of 0x100 to subaddress 0x10 would result in the data from RAM locations 0x100, 0x101, 0x102, 0x103 and 0x104 being supplied. Since the 1553 spec allows for up to 32 words of transmission per access to a given subaddress, a single access to subaddress 0x11 may transfer up to 32 words to the RAM.

Subaddress 0x12 provides access to a diagnostic register, unused in normal operation of the AFE. Subaddress 0x12 is read-only and gives a copy of the real-time clock implemented by the 1553 interface PLD for use with the microprocessor's temperature control loop. A bit in subaddress 0x12 is also reserved so that, if required, external 1553 software may poll subaddress 0x12 to see if the AFE microprocessor is busy or idle. This may be used to map the percentage of time the processor spends in the temperature control loop as opposed to command polling, allowing fine-tuning of temperature control parameters for optimal board performance.

4.2. Non-Standard 1553 Features

The AFE implements one non-standard 1553 feature. If external software performs a non-broadcast write cycle to the board, specifically with a word count of exactly 10 words (no more or less), and only to subaddress 0x15, then the board will reboot, performing a power-up reset. While this should never be necessary under any circumstances, the feature is added as a safety valve should some combination of temperature control parameters and/or command corruption somehow tie up the microprocessor such that it cannot respond.[7]

4.3. SVX Sequencer Bus Interface

The SVX Sequencer communicates with the AFE through a ribbon cable which lands upon the AFE Backplane. One cable actually contains two SVX control buses, and the backplane splits the signals such that each SVX cable services two adjacent AFE boards. Each SVX bus connection provides the following signals:

- 8-bit bidirectional SVX data bus
- DVALID signal driven from AFE to SVX Sequencer
- Differential SVX Clock
- Differential Crossing Clock
- CHANGE_MODE, MODE0 and MODE1 control lines to SVX

[7] The control room does, on occasion, appear to be infinite grad students typing on infinite keyboards.

- VCAL calibration voltage
- HDI_EN, FIRST_CROSSING, SYNC_GAP and CFT_RESET control signals

By and large the SVX Sequencer interface only controls the operation of the ~~SVX IIe~~ TRiP chips and the Virtual SVX logic of the AFE board. The discriminator function is essentially independent of the SVX operation, and data can still be driven out the LVDS cables even if the SVX Sequencer is disconnected. However, since the master timing of the AFE board is derived from the crossing clock as supplied on this cable, for the board to work as part of the detector system this link must be present and functional.

The design of the Virtual SVX provides for limited cross-coupling between the microprocessor and the SVX data bus such that SVX data may be sampled and read out over the MIL-STD 1553 bus and/or 1553 data appended to the SVX readout. This feature has rarely been explored in the AFE I and is likely to be removed in the AFE II to reduce cost.

4.4. Front Panel I/O, Test & Monitoring

The AFE has no front panel due to mechanical constraints. Because of the AFE's left-right symmetric design, an AFE inserted on either side of the mechanical cassette will have a pad pattern for an unstuffed backplane connector at the 'front'. Various surface mount LEDs will be visible when the board is installed, indicating power is present to the board. A pair of LEDs are placed near the front edge (actually a pair at each edge, only the pair to the front is stuffed, dependent upon handedness). This red/green pair is used to visually indicate whether the flex cable connection bayonet is fully inserted or not.

4.5. Rear Connector Interface

All AFE I/O occurs through the rear connector, to the backplane. The AFE connects to the backplane using two metric connectors from the series used for Compact PCI (e.g. AMP Z-Pack and/or equivalents from ERNI, FCI, etc.). One connector is a type 'A' which integrates 110 pins of connection with mechanical alignment features to insure the connector is aligned prior to pin mating. The other connector is a type 'B' which forfeits the alignment piece to provide 125 pins. Both connectors utilize top side shields which are used as extra ground returns. As can be seen in Tables 1 and 2 (pages 20 & 21), a large number of pins are ground and the grounds are arranged to provide good inter-signal isolation.

4.5.1. A Few Words About Ground

The AFE implements two 'grounds' on the PC board, a Digital Ground and an Analog Ground. The Analog one is meant to provide a less-noisy return for cryostat signals and A/D conversion circuitry. Various spots on the board near the converters allow the insertion of 0 ohm SMT resistors to tie the two grounds together at the converters. If none of the resistors are installed the two planes are isolated in the AFE. However, there is only one ground plane in the backplane – system ground – because the backplane is the star ground point from which all others radiate. When the AFE is plugged into the backpland the Analog Ground and the Digital Ground are automatically tied together in the backplane system ground plane. All metal in the cassette and cryostat is similarly grounded back to the backplane. A heavy braid ties the backplane ground plane to the detector ground.

All of the nasty digital signals possible are implemented as stripline between two planes of Digital Ground (with stitch vias around the perimeter) to act as shields. Similarly, all charge

inputs are implemented as striplines, surrounded by Analog Ground. Power planes are cut back such that they only extend over the areas actually using that power supply voltage, with the excess area in the power plane layers filled with extra layers of Ground, heavily tied to the "real" ground planes with numerous free vias.

Given that the AFE I is capable of individual photopeak detection from the Fiber Tracker, and that the 1 photoelectron peak is distinctly separated from the background, the AFE II shall not mess with success and no significant changes to the grounding scheme are planned.

4.5.2. Signal Descriptions

The various LVDS +/- signals are 370 MHz, Low-Voltage Differential Signaling standard, differential current source signals. They drive differential transmission lines and expect to see a termination equal to the characteristic impedance (typically 100 ohms) across the pair at the receiving end. The SLOTBIT signals are either left floating or tied to GND in order to give each AFE board a unique address for purposes of 1553 communication. The bits are a combination of slot position and a backplane address such that every AFE in the Central Fiber Tracker has a unique 1553 RT address.

All SVX signals are TTL level signals. All are inputs to the AFE except for DVALID and the SVX data bus. DVALID is an output from the AFE, and the SVX data bus is bidirectional.

4.5.3. Protocols

The LVDS data is continuous transmission with the data carried on the three data bits and the PLL of the LVDS receiver synchronized using the CLK lines in each link. Data on the LVDS links consists of 'frames', where one 'frame' is transmitted every 132 nsec. Each 'frame' consists of seven words of data. The most significant bit of the parallel data word issued by the receiver chip is used for synchronization, and is a copy of the crossing clock (high for one word, low otherwise). This acts as the 'start bit' for the frame.

SVX protocol consists of placing the SVX chip in one of four modes (Initialize, Acquire, Readout or Digitize) via use of the CHANGE_MODE, MODE0 and MODE1 lines. Dependent on mode, the SVX bus may be a data bus or individual control lines. The clock also changes speed in different modes. Please refer to the SVX II "Beginner's Guide" which may be found at

http://www-ese.fnal.gov/eseproj/svx/svx_htm/bgtsvx.htm

This document describes the 'generic' SVX II. The AFE II implements the standard Acquire/Digitize/Readout sequence, but as mentioned before, the TRiP chip may impact the Initialize methodology. The TRiP does not actually connect to the SVX interface; all SVX-like communication in the AFE is done using PLD logic.

5. ELECTRICAL & MECHANICAL SPECIFICATIONS

5.1. Packaging & Physical Size

The AFE is 14.435 inches high by 19.25 inches wide. It is a bare, 0.093" thick circuit board with no front panel. Components are mounted on both sides. Due to mechanical restrictions, component height above the board may be no more than 0.431" on the component side and no more than 0.050" on the solder side.

Pads on the back side of the AFE are used to mount back-side copper-beryllium springs to maintain spacing between the back side of the AFE and the metal plate of the cassette which holds the board. These springs also provide a solid electrical connection to insure that no cassette metal is electrically 'floating'.

5.2. PC Board Construction

Ten layer FR4 construction is used. Some gold plating is on the component side where the flex cables land; all other open surfaces are standard HASL finish. No ball-grid components are used on the AFE. The minimum pin-to-pin pitch is 0.5mm.

5.3. Power Requirements

Spreadsheet calculations indicate that the power dissipation should be approximately 34 Watts, split between +5V, +3.3V, ~~+5.5V~~ +3.3V (Analog) and ± 12V.[8] Local power regulation at each MCM insures minimal noise. The +3.3V (Analog) is used for the A/D chips and the TRiP chips, with the TRiP chips actually running at +2.5V, regulated down from +3.3V (analog).

5.4. Cooling Requirements

50 CFM airflow is provided by fans mounted below the backplane, providing airflow front-to-back. Normal bottom-to-top airflow is unavailable because the bottom is blocked by the cryostat and the top by the fiber optic cables entering the cassette.

[8] Later measurements show that the board actually runs about 36 Watts, with the wattage highly dependent upon the occupancy of the discriminator chips. The TRiP is expected to take less power than the SIFT did, so AFE II should run cooler than AFE I.

6. SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

Typical protection features such as temperature monitoring and power supply fusing are present on the AFE. The critical analog components are further insulated from power supply transients by the use of on-board linear regulators. Power dissipation has been minimized such that no component will dangerously overheat (e.g. to points of combustion) even if the fans fail; unassisted convection tests of physical heat models show that the air exit out the front is wide enough to accomplish this.

6.1. Module Fusing & Transient Supression

All power supplies entering the AFE from the backplane are fused on the AFE with fast-blow fuses. Transient suppression is handled by the bulk power supply.

6.2. Other Safety & Quality Assurance Subsections

The local microprocessor contains a built-in temperature sensor and continuously reports the temperature of the board. Bulk power supplies are remotely sensed at the backplane. The microprocessor also continuously monitors and controls the cryostat temperature. The total power available to the cryostat heater circuits is insufficient to cause damage to any component.